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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,698	05/19/2005	Martin Daum	CH02 0036 US	9253
65913	7590	09/05/2008	EXAMINER	
NXP, B.V.			MA, CALVIN	
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M/S41-SJ			ART UNIT	PAPER NUMBER
1109 MCKAY DRIVE				
SAN JOSE, CA 95131			2629	
NOTIFICATION DATE		DELIVERY MODE		
09/05/2008		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No. 10/535,698	Applicant(s) DAUM ET AL.
	Examiner CALVIN C. MA	Art Unit 2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 14 April 2008.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-7 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date _____

5) Notice of Informal Patent Application
6) Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade USP 6531996 in view of Shimada et al USP 5506598.

As to claim 1, Murade teaches a LC-Display (200) with n gate drivers (104) and a source drivers (i.e. the data line driving circuit) for driving the LC-Display with dots arranged in x rows and y columns (i.e. the active matrix LCD panel consists of x rows and y columns) (see Fig. 1, Col. 13, Lines 18-67), wherein the gate drivers has-comprises several output stages for driving the gate lines of the LC- Display (i.e. the gate driver has two side each controlling the individual lines, therefore comprises several output stages (see Fig. 1), the LC-Display comprising:

a gate on supply line VH to turn on a transistor of the LC-Display (i.e. voltage VDDY which drive the right side 104 scanning line driving circuit and can turn on the transistors under the proper control switching) (see Fig. 1, Col. 13, Lines 6-38);

a gate off supply line VL to turn off a transistor of the LC-Display (i.e. voltage VSSY which drive the left side 104 scanning line driving circuit and can turn off the transistors under the proper control switching), wherein the Gate off supply line VL;

a circuit to connect a storage capacitance Cst of a selected Rate line GLy to keep other storage capacitors Cst of unselected gate lines connected to the gate off supply line VL (i.e. the gate lines are all connected to the matrix array which serve as a capacitor Cst in storing the electrical charges) (see Fig. 1).

However, Murade does not explicitly teach an additional gate off supply line VLclean is to substantially reduce a discharge time associated with driving transistors of the LC-Display, wherein the additional gate off supply line is coupled to the output stages of the gate drivers and is routed as a separate track from the Rate off supply line VL; and

Shimada teaches an additional gate off supply line VLclean is to substantially reduce a discharge time associated with driving transistors of the LC-Display, wherein the additional gate off supply line is coupled to the output stages of the gate drivers and is routed as a separate track from the Rate off supply line VL (i.e. the second gate line 101b in each of the vertical control lines are used to turn the circuit off and for the purpose of improving performance) (see Fig. 2, Col. 3, Lines 1-28); and

Therefore it would have been obvious for one of ordinary skill in the art at the time the invention was made to have used the double control line design of Shimada in the overall LCD circuitry of Murade in order to reduce the off current (see Shimada Col. 2, Lines 22-24).

As to claim 2, teaches the LC-Display as claimed in claim 1 wherein the output stage comprises:

a PMOS transistor (202b) MP1 arranged between the gate on supply line VH and an output of the output stage; and

a first NMOS transistor MN1 (202a) arranged between the gate off supply line VL and the output of the output stage; and

a second NMOS transistor MN2 (202a) is arranged between the additional gate off supply line VLclean and the output of the output stage (i.e. the Precharging mechanism which is between the gate driver and the output stage can be created with a series of complementary TFT which include both N-channel and P-channel functionality) (see Fig. 4, Col. 16, Lines 60-67).

As to claim 3, Shimada teaches the LC-Display as claimed in claim 1, wherein the additional gate off supply line VLclean is routed over a separate track on the LC-Display glass (i.e. the two lines 101a and 101b are clearly routed over a separate track) (see Fig. 2).

As to claim 4, Shimada teaches the LC-Display as claimed in claim 1, wherein a track of the gate off supply line VL and a track of the additional supply line VLclean are coupled to a same supply level (i.e. since the two voltage supply line create the differential voltage from the graph in figure 7 both of the line can have the same level) (see Fig. 7).

As to claim 5, Shimada teaches the LC-Display as claimed in claim 1, further comprising a power supply to supply a voltage to the gate off supply line VL and the additional gate off supply line VLclean, wherein a track of the gate off supply line VL and a track of the additional gate off supply line VLclean are connected together in a location wherein a track impedance to an output of the power supply is relatively low (i.e. since both of the off supply line are from the same TFT layer they have relatively low impedance where the overall display power supply ultimately supply the lines together) (see Fig. 2, Col. 2, Lines 1-42).

As to claim 6-7, see discussion of claim 2 above, claim 6-7 is analyze to have a broader scope then claim 2 and is rejected for the same reason.

Response to Arguments

3. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CALVIN C. MA whose telephone number is (571)270-1713. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on 571-272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Calvin Ma

/Chanh Nguyen/

Application/Control Number: 10/535,698
Art Unit: 2629

Page 7

August 28, 2008

Supervisory Patent Examiner, Art
Unit 2629